Photonic Combinatorial Network for Contention Management in 160 Gb/s-Interconnection Networks Based on All-Optical 2×2 Switching Elements

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***Abstract*—A modular photonic interconnection network based on a combination of basic 2×2 all-optical nodes including a photonic combinatorial network for the packet contention management is presented. The proposed architecture is synchronous, can handle optical time division multiplexed (OTDM) packets up to 160 Gb/s, exhibits self-routing capability, and very low switching latency. In such a scenario, OTDM has to be preferred to wavelength division multiplexing (WDM) because in the former case, the instantaneous packet power carries the information related to only one bit, making the signal processing based on instantaneous nonlinear interactions between packets and control signals more efficient. Moreover, OTDM can be used in interconnection networks without caring about the propagation impairments because of the very short length (< 100 m) of the links in these networks. For such short-range networks, the packet synchronization can be solved at the network boundary in the electronic domain without the need of complex optical synchronizers. In this paper, we focus on a photonic combinatorial network able to detect the contentions, and to optically drive the contention resolution block and the switching control block. The implementation of the photonic combinatorial network is based on semiconductor devices, which makes the solution very promising in terms of compactness, stability, and power consumption. This implementation represents the first example of complex photonic combinatorial network for ultrafast digital processing. The network performance has been investigated for bit streams at 10 Gb/s in terms of bit error rate (BER) and contrast ratio. Moreover, the suitability of the 2×2 photonic node architecture exploiting the earlier mentioned combinatorial network has been verified at a bit rate up to 160 Gb/s. In this way, the potential of photonic digital processing for the next generation broad band and flexible interconnection networks has been demonstrated.**

***Index Terms*—Broad-band interconnection networks, nonlinear optics, optical packet switching, optical signal processing.**

I. Introduction

HIGH speed communication and processing are key features for future ultrafast transmission and computing systems, within scenarios ranging from wide-area backbone networks to interchip interconnection networks. In backbone networks, router capacity increase is being limited by the difficulties of achieving ultrahigh speed packet processing and switching in the electronic domain. In particular, the most relevant issues concern the limit of the memory speed, the bottleneck of the packet arbitration, and the complexity of the interconnections [1]. In interconnection networks enabling ultrahigh speed interchip communication in high performance computing systems, current electronic solutions are also approaching their fundamental limitations in terms of power, wiring density, and throughput [2].

Till date, optics has been extensively used to increase channel capacity in enterprise data links and service provider transmission networks, by exploiting optical time and wavelength division multiplexing techniques (OTDM/WDM) [3]. The main reasons of the success of photonic technologies are: ultrahigh transmission speed, high signal transparence degree, low power consumption, and electromagnetic field immunity.

In order to achieve the required ultra wide-bandwidth and low-latency data processing, optical solutions for signal processing are gaining increasing interest [4], at least at the research stage. Indeed, some interesting solutions have been proposed for realizing optical switches and logic gates based on optical fibers [5]–[10], semiconductor devices [11]–[19], or waveguides [20]. Moreover, several research efforts have been undertaken in order to demonstrate the suitability of new schemes for the realization of optical logic gates [21], [22]. Few examples of the simple cascade of two logic gates have been demonstrated [23], [24], while the design and the implementation of more complex digital circuits involving cascades of several logic functions have not been addressed yet.

In a previous work [25], we proposed a reconfigurable and integrable optical logic gate based on a semiconductor optical amplifier (SOA). Here, we demonstrate the implementation of a complex combinatorial network by simply cascading various replicas of such SOA-based logic gates. This combinatorial network can be used for contention management in a 2×2 photonic node architecture, where all the forwarding functions (label recognition and processing, contention detection and resolution, switch control, switching, and regeneration) are optically performed by exploiting integrable solutions.

Thanks to the full all-optical processing, the packet latency time due to the switching approaches the passing-through time of light in the photonic switch (few nanosecond, even less than one nanosecond if optical integration can be achieved). The low latency, together with the high scalability, makes the 2×2 all-optical node suitable as a switching element

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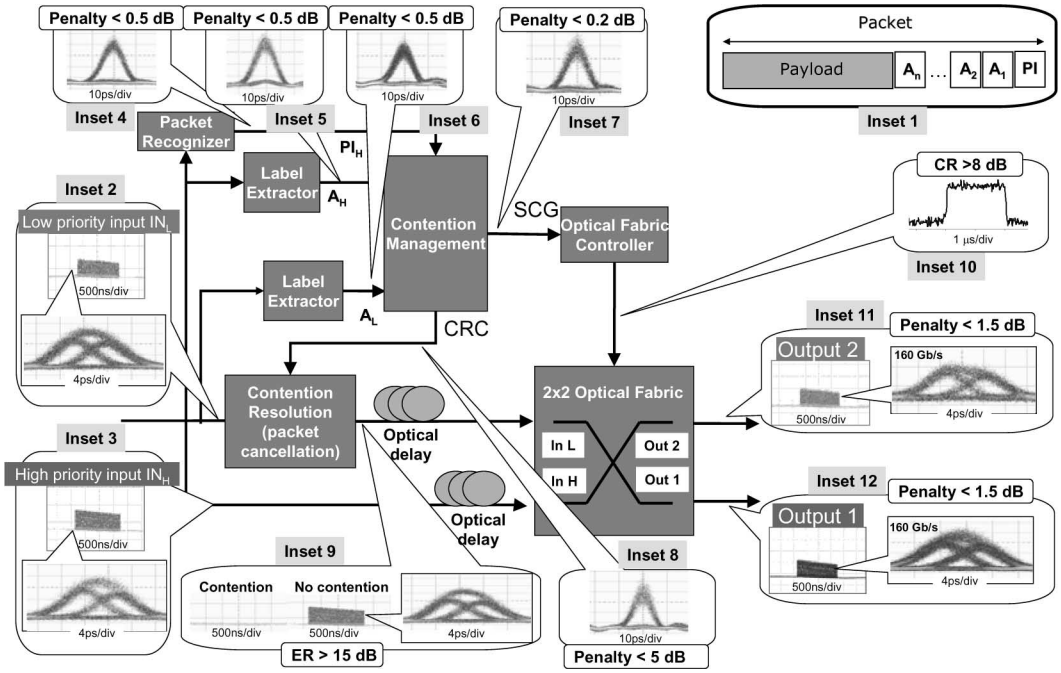

Fig. 1. Photonic node architecture and packet format (inset 1). A_H: high priority packet address bit; PI_H: high priority packet identifier bit; A_L: low priority packet address bit; OUT 1 identified by address '0'; OUT 2 identified by address '1'; CRC: contention resolution control; SCG: switching control generation.

in short-range multistage interconnection networks, aimed at connecting processors and memories of a high-performance computing cluster. Indeed, in such a short-range scenario the network synchronization can be easily maintained, and the absence of effective optical buffers is less problematic.

However, several challenging issues are open, since advanced processing functionalities have not been performed yet. In this sense, the implementation of complex photonic combinatorial networks represents a fundamental and promising stage in the optical network evolution. Moreover, the proposed photonic node architecture represents a demonstration of the feasibility of ultrafast photonic interconnection networks, which can be improved by moving toward integrated implementations of each subsystem.

The paper is organized as follows: Section II describes the architecture of the proposed 2×2 photonic node, while Section III introduces multistage interconnection networks that perfectly fit this switching element. The scheme and the implementation of the photonic combinatorial network for the contention management into the node are reported in Section IV and V respectively. Finally, the suitability of all 2×2 photonic node subsystems to process 160 Gb/s packets is demonstrated in Section VI.

II. 2×2 Photonic Node Architecture

In this section, we describe the architecture of the proposed 2×2 photonic node, shown in Fig. 1, and the implementation of each subsystem.

The 2×2 switching element operates synchronously on fixed length packets. The switching operation is achieved by means of ultrafast digital processing in the optical domain, exploiting nonlinear effects in nonlinear devices. This approach makes optical time division multiplexing (OTDM) preferred to wavelength division multiplexing (WDM). In fact, in the former case, the instantaneous packet power carries the information related to only one bit, which can be recognized by exploiting the instantaneous interaction between packet and control signal. In the WDM case, the coexistence of several spectral components, each one carrying a bit stream, makes the optical packet processing considerably more complex and less efficient. OTDM can be used, in this scenario, without caring about the propagation impairments, since the links of the interconnection networks are very short (< 100 m). In such short-range networks, the packet synchronization can be solved at the network boundary in the electronic domain, without the need of complex optical synchronizers.

Since all the node operations and processing occur in the photonic domain, a simple label structure has been adopted. In this way, the complexity of the all-optical packet processing is reduced, and the packet self-routing in multistage node combinations is simplified. As shown in Fig. 1 (inset 1), the first bit PI (packet identifier) of the packet allows the packet recognition, while the path is defined associating the ith switch with the ith bit L_i of the label. Each bit of the label is read in the optical domain by exploiting nonlinear effects in semiconductor devices. The processing time in this case is less than 10 ns, and it is limited by the propagation delay in the fiber pigtails. The contention detection is performed through the combinatorial network described in Section III. Then, the contention is resolved by the cancellation (i.e., dropping) of contention-losing packets. The bar or cross state of the 2×2 fabric is set by means of a control signal represented by an optical gate [26]. This gate lasts as long as the packet duration, and depending on its high or low power level, nonlinear effects occur or do not occur,

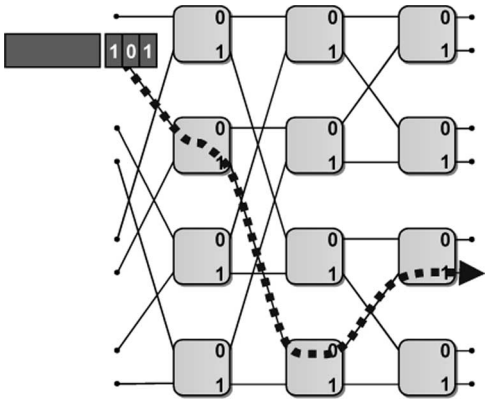

Fig. 2. Multistage Banyan-based all-optical interconnection architecture.

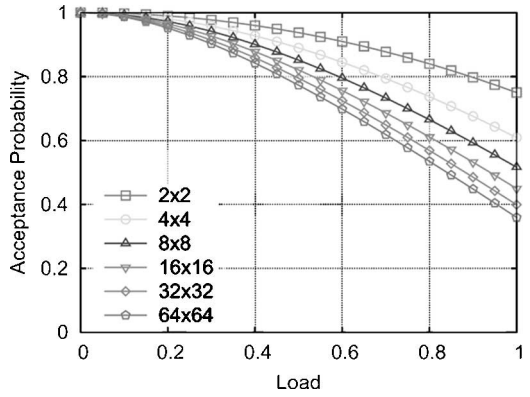

Fig. 3. Packet acceptance probability in the multistage Banyan-based all-optical interconnection architecture.

respectively, in the 2×2 fabric. The packets are consequently switched to the proper output [27]. The switching time defined as the time needed to pass from 10% to 90% of the total swing is lower than one bit time and it is limited by the transients of the switching control signal.

III. Multistage Interconnection Networks

Cascading of the basic 2×2 node can be arranged by resorting to multistage interconnection networks already present in the literature. To benefit from the self-routing property, a Banyan topology [28], [29] has been selected. An example of an 8×8 Banyan network is shown in Fig. 2. The routing in such a topology perfectly fits the proposed 2×2 node architecture: in fact, as shown in the picture, every switching element in stage i just needs to look at ith bit in the packet header in order to perform the switching decision. However, the Banyan switching matrix is internally blocking, i.e., collisions between packets directed to different output port may occur within the interconnection network. This condition limits the throughput especially for large networks, as shown in Fig. 3. Nevertheless, internal blocking can be avoided by presenting the packets at Banyan network input ports for ascending header values. To properly sort the packets, the Banyan network can be preceded by a Batcher network, as shown in Fig. 4 [29]. From the implementation standpoint, the elements of the Batcher network

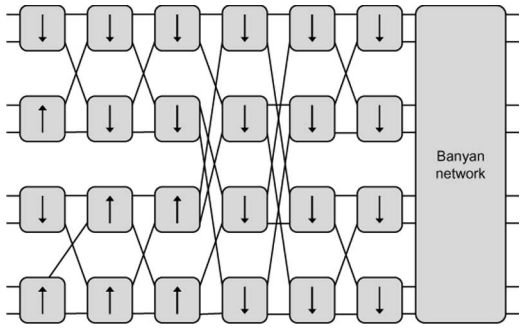

Fig. 4. Batcher–Banyan network configuration.

make slightly more complicate switching decisions: they route the packets sending the ones with higher address value to a predefined output port (upper or lower port depending on the arrow direction in Fig. 4). In this case, a magnitude comparison involving all the address bits apart from a single bit comparison is performed by the switching element.

IV. Combinatorial Network for Contention Management

All-optical packet contention management is addressed by means of a combinatorial network designed to process label information in order to properly configure the 2×2 all-optical switching node, and to drive the contention resolution block. With reference to Fig. 1, the following hypotheses are considered: 1) the two switching input ports have different priority (H: high, and L: low); 2) the packets synchronously reach the input ports, and have the same time duration; and 3) the packet label is composed of one PI bit and an N-bit address where each bit refers to one of N network stages, and its value univocally determines the packet route ('0' identifies output port 1 and '1' identifies output port 2 of the incoming switch).

Once the packet reaches the high priority input port, Label Extractor and Packet Recognizer block isolate the address bit $\mathrm{A_H}$ and the $\mathrm{PI_H}$ bit, respectively, where subscript H stands for high priority. If the packet enters low priority input port, it is processed only by the label extractor in order to extract the address $\mathrm{A_L}$, where L stands for low priority. The PI is not necessary for low priority input port, this port being conditioned by the high priority input. $\mathrm{A_H}$, $\mathrm{A_L}$, and $\mathrm{PI_H}$ form the input signals for the combinatorial network whose outputs are the switching control generation (SCG) and contention resolution control (CRC) signals. The former is responsible for switching bar/cross configuration, the latter drives the contention resolution block.

For proper operation, the combinational network must preserve the packet incoming from the high priority input ($\mathrm{PI_H} = 1$) and send it to the correct output port indicated into the address ($\mathrm{A_H}$). At the same time, if contention is detected ($\mathrm{CRC} = 1$ when $\mathrm{A_H} = \mathrm{A_L}$), it must be resolved by the devoted block. On the other hand, when $\mathrm{PI_H} = 0$ (high priority input packet not present), the low priority packet must be redirected to the proper output port ($\mathrm{A_L}$). If we associate the values '0' and '1' of the SCG to the switch cross and bar states, respectively, the truth table for the combinatorial network results as shown in Fig. 5.

A_H	A_L	PI_H	CRC	SCG
0	0	0	**0**	**0**
0	0	1	**1**	**1**
0	1	0	**0**	**1**
0	1	1	**0**	**1**
1	0	1	**0**	**0**
1	1	1	**1**	**0**
1	0	0	**0**	**0**
1	1	0	**1**	**0**

Impossible cases

Fig. 5. Combinatorial network truth table: CRC $= 0$ no contention; CRC $= 1$ contention occurs; SCG $= 1$ switch in bar configuration; SCG $= 0$ switch in cross configuration.

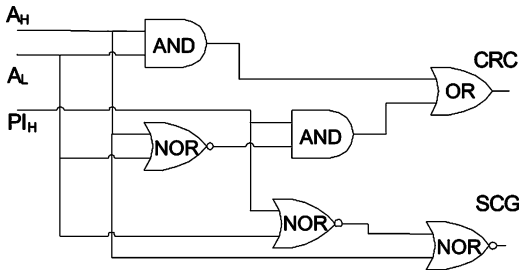

Fig. 6. Logic circuit representing the combinatorial network for the contention management.

As first example, we consider the case $\mathrm{PI_H} = 0$: it means that the packet is not present at the high priority input. Thus, physically the value for the corresponding address bit $\mathrm{A_H}$ is '0'. For what concerns the low priority input, $\mathrm{A_L} = 0$ states that the packet does not exist or that it must be routed to the output port '0'. In this case, no contention occurs (CRC $= 0$), and the switch must be set in the cross state (SCG $= 0$). If $\mathrm{PI_H} = 1$ and both the addresses $\mathrm{A_H} = \mathrm{A_L} = 0$, a contention is detected (CRC $= 1$), and the circuit must guarantee the priority to the high priority input. This means bar configuration for the switch (SCG $= 1$). All the other cases can be easily determined following the previous examples. The truth table also contains two cases without physical sense: in fact, when $\mathrm{PI_H} = 0$, no input packet flows through high priority port, and therefore, $\mathrm{A_H}$ can not assume the value '1'.

The combinatorial network can be obtained by implementing the logic circuit in Fig. 6, where the following logic gates are used: three NOR, two AND, and one OR. For this logic circuit we exploit a SOA-based implementation, which gives benefits in terms of compactness, stability, and power consumption. One AND function is based on four wave mixing (FWM) in an SOA. Two NOR functions are realized by means of cross gain modulation (XGM) induced in SOAs by the input signals on an auxiliary counterpropagating channel (AUX). The cascade of one NOR and one AND function is obtained by means of XGM induced in SOA by two input signals on a third counterpropagating input signal. Finally, the OR function is realized simply using a 3-dB coupler: this is possible just because its input ports can not be '1' at the same time. Since the signals fed into the 3-dB coupler must be at the same wavelength, a wavelength converted copy ($\mathrm{PI_C}$) of $\mathrm{PI_H}$ is obtained by FWM in SOA using the auxiliary channel. The physical schematic setup is shown in Fig. 7.

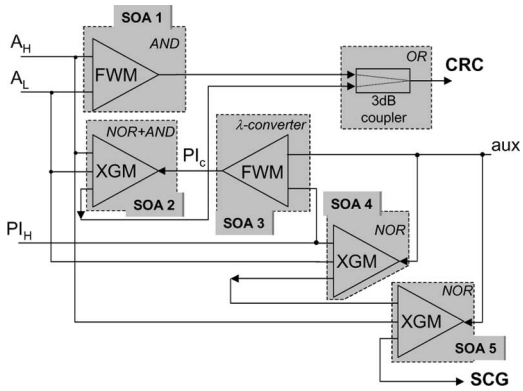

Fig. 7. Physical schematic setup: triangles represent SOAs (exploited effect indicated inside); aux: probe signal; $\mathrm{PI_C}$: wavelength converted $\mathrm{PI_H}$.

V. Combinatorial Network Implementation

The practical implementation with discrete devices brings to the experimental setup in Fig. 8. The input signals $\mathrm{A_H}$ and $\mathrm{PI_H}$ are generated by means of a mode-locked fiber laser producing 10-ps-optical pulses at a repetition rate of 10 GHz and wavelength $\lambda_\mathrm{H} = 1550.9$ nm. In order to evaluate the performances of the logic circuit, a pseudo-random bit sequence (PRBS) $2^7 - 1$ is mapped onto the pulses by means of a Mach–Zehnder modulator. $\mathrm{A_L}$ is an uncorrelated wavelength converted ($\lambda_\mathrm{L} = 1552.5$ nm) replica of $\mathrm{A_H}$. $\mathrm{A_H}$ and $\mathrm{A_L}$ are fed into SOA1, both with a power of 9.6 dBm. They interact in SOA1 generating an FWM signal at the new wavelength $\lambda_\mathrm{CRC} = 2\lambda_\mathrm{H} - \lambda_\mathrm{L} = 1549.3$ nm, which represents the outcome of the AND function. The same signals, both with a power of 5 dBm, interact in the SOA2 inducing XGM to the counterpropagating signal $\mathrm{PI_C}$ (the power of $\mathrm{PI_C}$ is -2.5 dBm). $\mathrm{PI_C}$ is a wavelength converted replica of $\mathrm{PI_H}$ obtained through FWM in the SOA3 between $\mathrm{PI_H}$ and a pulse train (AUX) at $\lambda = \lambda_\mathrm{L} = 1552.5$ nm. In this way, the signal which counterpropagates in SOA2 has the same wavelength as the FWM at the output of SOA1. Therefore, they can be coupled together in order to give the CRC output. No interference occurs at this coupler because two logic 1 inputs are not allowed.

SCG is obtained by exploiting XGM in SOA4 and SOA5, where NOR logic functions are implemented. The power at SOA4 input is 4.7 dBm for $\mathrm{PI_H}$, 2.5 dBm for A_L, and -19.5 dBm for the counterpropagating AUX. SOA5 input powers are: 8.8 dBm for $\mathrm{A_H}$, 5.2 dBm for the signal coming from SOA4, and -14.2 dBm for the counterpropagating AUX.

SOAs saturation level is biased through a continuous wave (CW) signal at a wavelength of $\lambda_\mathrm{CW} = 1540$ nm. The CW is injected, with the following input powers, copropagating with respect to the output signal as: 11.5 dBm (SOA1), -2.9 dBm (SOA2), 10.9 dBm (SOA3), 3.5 dBm (SOA4), and 14.5 dBm (SOA5). The maximum average power that we need to exploit nonlinear effects in the SOAs is 9.6 dBm. Such power values can

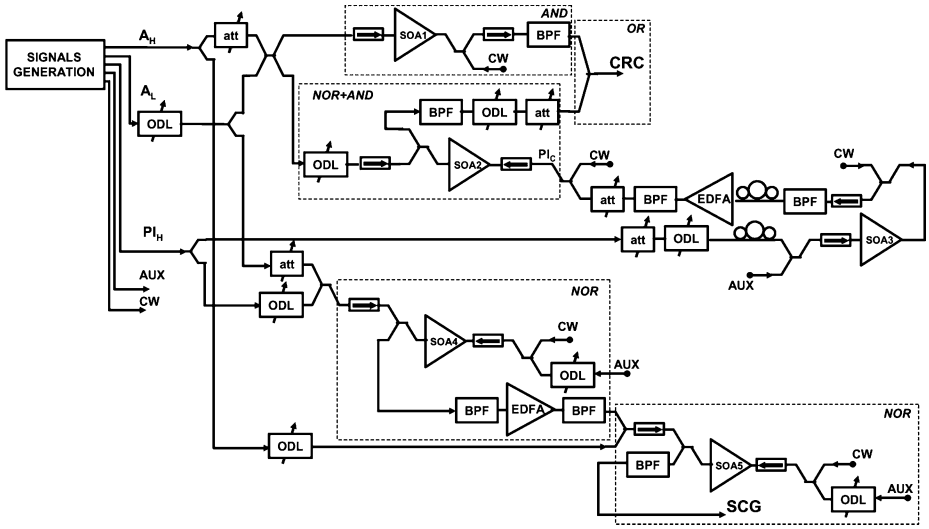

Fig. 8. Experimental setup. Connections for AUX and CW signals are not represented for clearness.

be easily obtained by means of low-power erbium-doped amplifiers. In case of integrated realization, erbium-doped waveguide amplifiers can be used.

Note that we used five different discrete SOAs with saturation output power in the range 6–14 dBm, optical gain in the range 18–25 dB, and noise figure in the range 8–10 dB. An integrated implementation based on identical SOAs would allow reducing the costs, the complexity, and the power consumption of the scheme. Tunable optical delay lines (ODL) and 0.3-nm-optical band-pass filters are used in order to properly synchronize and select the involved signals.

The main performances for the combinatorial network are summarized in Figs. 9 and 10, where the sequences and the eye diagrams for the three input signals and for the two output signals are shown, respectively. SCG and CRC sequences reveal that the logic circuit works properly, i.e., according to the truth table in Fig. 5. The output sequences are not perfectly equalized due to residual patterning effect, but the contrast ratio (CR) between high and low level is between 8 and 9.3 dB for the SCG and between 8.4 and 10 dB for the CRC. These values could be further improved by using well-known pedestal suppressor schemes [30]. The eye diagrams of the output signals look sufficiently clear, thus, confirming the good performance of the implemented combinatorial network.

BER measurements are performed in order to evaluate the effectiveness of the logic operations and the noisiness of the output signals (Fig. 11). The measurements are performed after a preamplified receiver. At BER $= 10^{-9}$, a negligible penalty is present for the SCG and a 5-dB-power penalty is present for the CRC that can be mainly ascribed to the noise arising during the FWM process in SOA1 and SOA3.

A 5-dB penalty can be accepted because the CRC at the output of the combinatorial network is used only in the node where it is generated for driving the contention resolution block, according to its high or low value. We stress that it has not to be transmitted to the following nodes. The SCG is used within the same node where it is generated as well, and the signal quality must be sufficient for driving the fabric controller.

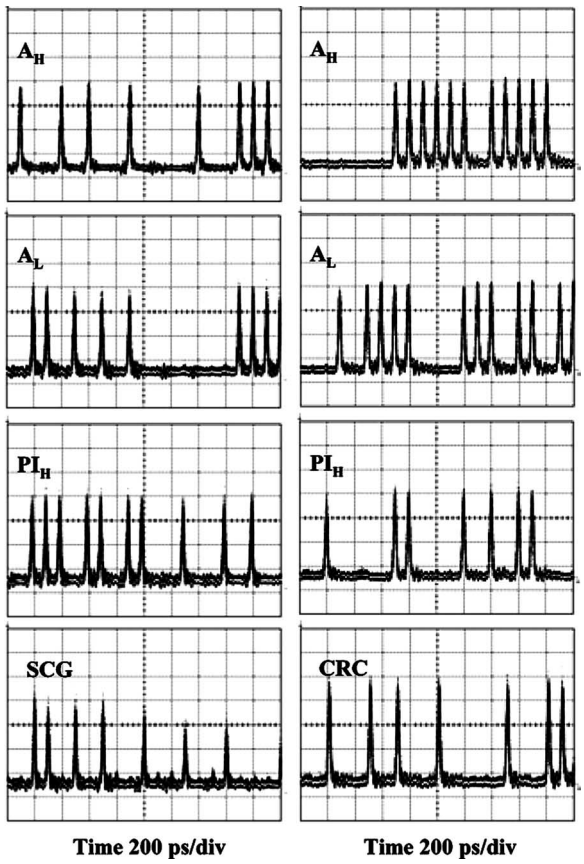

Fig. 9. Input sequences and corresponding SCG and CRC output signals.

VI. Feasibility Demonstration of the Subsystems of the 2×2 Photonic Node at 160 Gb/s

An experimental validation of all the 2×2 photonic node subsystems has been carried out by considering compact solutions

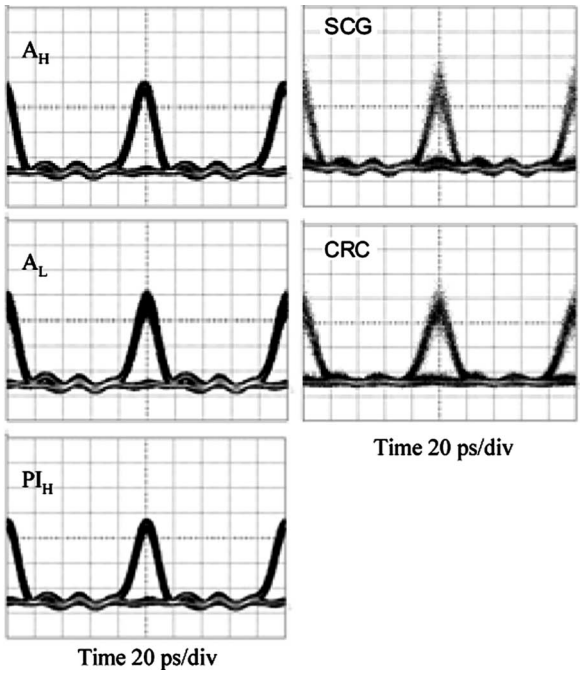

Fig. 10. Input eye diagrams for A_H, A_L, and PI_H (left) and output eye diagrams for SCG and CRC (right) in the case of BER $= 10^{-9}$. The input sequences are $2^7 - 1$ PRBS.

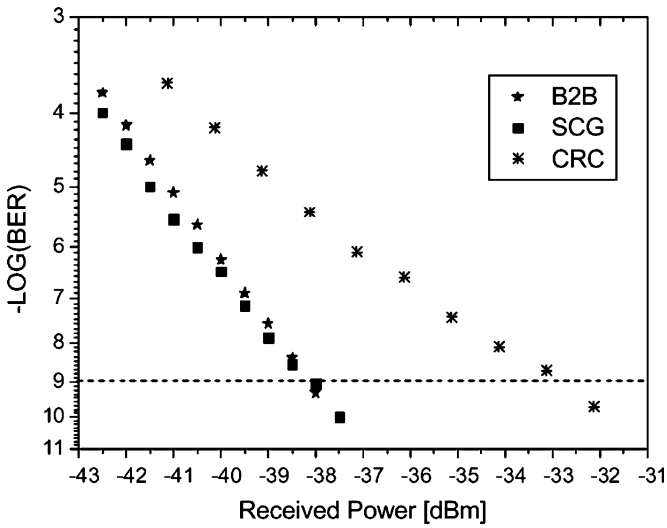

Fig. 11. BER measurements for back-to-back (B2B), SCG, and CRC. Input sequences are $2^7 - 1$ PRBS.

that can be partially or fully integrated. Their performance has been evaluated using OTDM signals up to 160 Gb/s, which are obtained by time-interleaving of 2-ps-pulse trains at 10 Gb/s. These pulse trains are generated by a mode locked fiber laser. In this way, we demonstrated that the proposed node can successfully process packets at this high bit rate. In Fig. 1 (inset 2 and 3) the input packets and the eye diagram of the 160 Gb/s payloads are reported. In order to be able to estimate the quality of the 160 Gb/s eye diagram using a 50-GHz-bandwidth oscilloscope, we turned on just two adjacent tributary channels. As a consequence, the instrument impulsive response allows to distinguish the high quality of the signal. Concerning the label processing, the experimental setup includes a packet recognizer and a label extractor based on FWM in SOA. The pump inducing the nonlinear phenomenon is represented by a pulse train with a repetition rate equal to the packet rate (100 kHz in this case). Each pulse is synchronized with the packet recognition bit for the packet recognizer block, and with the bit corresponding to the switch address for the label extractor block. It has been demonstrated that FWM-based processing in SOA allows elaborating signals up to 160 Gb/s with a penalty less than 0.5 dB (at BER $= 10^{-9}$). This performance is reported in Fig. 1 (inset 4–6) where the eye diagrams of the signals at the output of the blocks for packet recognition and label extraction are reported. The eye diagrams are taken with a 50-GHz-bandwidth oscilloscope.

In the literature, the contention management block represents one of the more immature subsystems, because it requires complex logic operations. In our case, we designed the above mentioned photonic combinatorial network able to generate two different outputs: CRC for driving the contention resolution block, and SCG for driving the 2×2 fabric controller. Here we verified the suitability of the proposed solution for processing packets up to 160 Gb/s.

In Fig. 1 (inset 7 and 8), the eye diagram of the two signals at the output of the combinatorial network as displayed by the 50-GHz-bandwidth oscilloscope together with the corresponding penalties is shown.

In the proposed architecture of the 2×2 photonic node, the contention resolution requires the cancellation of the low-priority packet. This cancellation is obtained by means of XGM in SOA induced by a pump gate as long as the packet duration ($2\ \mu$s). In this case, we obtain an extinction ratio (ER) defined as the ratio between the power at the output of the block in case of absence and in case of presence of contention, higher than 15 dB, as shown in Fig. 1 (inset 9). In the same inset, we can also see the eye diagram of the low-priority packet payload in case of contention absence obtained with the 50-GHz-bandwidth oscilloscope. The pump gate can be generated starting from the input CRC pulse exploiting an all-optical flip-flop. The flip-flop is placed in the contention resolution block. Another flip-flop can be used in order to produce the control gate that determines the bar or cross configuration in the optical switch. In fact, the 2×2 fabric controller also has to generate an optical gate as long as the packet length, starting from the input SGC pulse. This flip-flop is placed in the optical fabric controller. In the literature [31]–[33], few solutions for the implementation of an all-optical flip-flop are reported. Our implementation [26] is based on a new scheme, which presents benefits in terms of complexity, stability, switching time, and wavelength independence in the C-band. It exploits the absorption and emission properties of an erbium-doped fiber acting as an optical flip-flop, when proper input conditions are applied. In particular set and reset pulses, if properly chosen in spectral regions where the absorption and the gain dominate respectively, can induce transparency and opaqueness in the active medium.

This property allows to control the output power level of a CW probe signal, as shown in Fig. 1 (inset 10). The solution exhibits transition times of about one picosecond, gate duration of several microseconds, and a contrast ratio between the high and low output power higher than 8 dB. A more compact scheme can be obtained by applying the same principle to a doped waveguide.

Concerning the optical switching operation, to the best of our knowledge, few optical technologies are capable of ultrashort switching time (< 100 ps), and among them SOAs and nonlinear fiber-based switches are the most promising candidates [11], [34], [35]. The latter ones are fast enough to operate at ultrahigh speed but they cannot be integrated. On the other hand, the SOA-based switches show good performance in terms of compactness, stability, cost and power requirements, but they present some limitations concerning the maximum operating bit rate. Recently, the new generation of ultrafast SOAs, together with the use of several technique to make these devices suitable in ultrafast applications [25], is allowing efficient signal processing. Moreover, the use of complex interferometric architectures is avoided, and the compactness and stability of the optical schemes are increased at the same time. In our case, the optical switching operation has been achieved by exploiting XGM in a single SOA [27], obtaining spatial and wavelength preserving 2×2 switches. Fig. 1 (inset 11 and 12) reports both output packets and their eye diagram in the case of 2×2 fabric bar configuration, as visualized by a 50-GHz-bandwidth oscilloscope. The pulse width of both output signals is lower than 3 ps as measured by an autocorrelator. The performance is similar for input packet wavelengths in the range 1540–1555 nm, with penalties lower than 1.5 dB, which make this scheme suitable for cascade configurations. Moreover, if long cascade are envisaged, optical regenerators able to compensate for all distortions due to the optical processing in the nodes can be periodically inserted every n switches, where n depends on the quality of the receivers used in the interconnection network. The optical regeneration has already been demonstrated for packets up to 160 Gb/s [36].

For what concerns the power constraints, the average power of the packets at the output of the 2×2 fabric depends on the saturation power of the employed SOAs. The output power can be as high as 7 dBm with SOAs with output saturation power of 14 dBm. The required power for the packets at the input of the 2×2 fabric is lower than 2 dBm [27], giving a minimum power margin of 5 dB. This margin allows propagating the signal along a span up to 25 km. Therefore, it is a wide margin in case of short-range (< 100 m) applications. It has been shown in Section V that the maximum average power needed for the signals in the combinatorial network was 9.6 dBm at SOAs input. In an implementation with discrete component, these values can be easily reached with low power EDFAs placed at the input of the combinatorial network. In an integrated implementation, the use of erbium-doped waveguide amplifiers allows reaching the necessary input power. Therefore, the high scalability of the 2×2 photonic node is also guaranteed from the power requirements standpoint.

VII. Conclusion

A complex photonic combinatorial network for packet contention management in optical packet switching networks has been proposed for the first time to the best of our knowledge. The proposed scheme is able to drive contention resolution and switching control blocks by processing optical packets up to 160 Gb/s. Moreover, an SOA-based implementation makes the solution very attractive for its potentialities in terms of integration, stability, and low power consumption. BER measurements for bit streams at 10 Gb/s confirm the effectiveness of this logic circuit. The combinatorial network has been used to manage the packet contention in a synchronous 2×2 photonic node, which can handle ultrafast OTDM packets up to 160 Gb/s, and exhibits self-routing capability and very low switching latency. This kind of switching element well fits as a basic block of multistage interconnection network architectures aimed at connecting processors and memories of a high-performance computing cluster. Indeed, in such a short-range scenario, the packet synchronization issues can be solved at the network boundary in the electronic domain, and the transmission impairments due to the packet high bit rate can be neglected. Finally, a validation of all subsystems of the proposed 2×2 photonic node at 160 Gb/s confirms the suitability and the potentialities of photonic digital processing for next generation broad-band communication networks.

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